Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

1. (Previously Presented) A system for recovering timing information from a received serial data signal, comprising:

a phase interpolator adapted to produce a data sampling signal and a phase sampling signal each having an interpolated phase responsive to a plurality of phase control signals, wherein the phase sampling signal is offset in phase relative to the data sampling signal by a predetermined amount;

a data path that samples the received serial data signal according to the data sampling signal to produce a data signal;

a phase path that samples the received serial data signal according to the phase sampling signal to produce a phase signal;

a phase detector that produces a phase error signal based on the data signal and the phase signal, wherein the phase error signal is indicative of a phase offset between the data sampling signal and the received serial data signal;

a phase error processor that produces a rotator control signal based on short-term error processing and long-term error processing of the phase error signal; and

a phase control signal rotator adapted to rotate the plurality of phase control signals and correspondingly the interpolated phases of the data sampling and the phase sampling signals in response to the rotator control signal.

2. (Previously Presented) The system of claim 1, wherein the phase error processor is adapted to cause the phase control signal rotator to rotate the plurality of phase control signals and correspondingly the interpolated phase of the data sampling signal and the phase sampling signal in a direction to reduce the phase offset between the received serial data signal and the data sampling signal.

3. (Currently Amended) The system of claim 1, wherein the rotator control signal is one of a phase-advance, a phase-retard, and a phase-hold signal, the phase control signal rotator being adapted to:

rotate the plurality of phase control[[s]] signals in a first direction to advance the interpolated phase of the data sampling signal and the phase sampling signal in response to the phase-advance signal;

rotate the plurality of phase control[[s]] signal in a second direction to retard the interpolated phase of the data sampling signal and the phase sampling signal in response to the phase-retard signal; and

prevent the plurality of phase control signals and correspondingly the interpolated phase of the data sampling signal and the phase sampling signal from rotating in response to the phase-hold signal.

4. (Previously Presented) The system of claim 3, wherein the phase control signal rotator includes a ring of storage elements each adapted to store one of the plurality of phase control signals, the rotator being adapted to:

concurrently shift in the first direction each of the phase control signals from a present storage element to an adjacent storage element in response to the phase-advance signal; and

concurrently shift in the second direction each of the phase control signals from the present storage element to an adjacent storage element in response to the phase-retard signal.

5. (Previously Presented) The system of claim 1, wherein each of the plurality of phase control signals is a digital signal.

6. (Previously Presented) The system of claim 1, wherein the phase control signal rotator is a circular shift register including one of:

a plurality of linearly arranged storage cells each adapted to store a respective one of the plurality of phase control signals; and

a plurality of storage cells arranged in a matrix of rows and columns and linked together to form a ring structure, each of the storage cells being adapted to store a respective one of the plurality of phase control signals.

7. (Previously Presented) The system of claim 1, wherein the control signal rotator is adapted to cause the phase interpolator to rotate the interpolated phase of the data sampling signal and the phase sampling signal to one of a plurality of discrete phase values spanning a phase range of 360°.

8. (Canceled)

9. (Previously Presented) The system of claim 1, wherein the phase error processor and the phase control signal rotator are adapted to cause the phase interpolator to rotate the data sampling signal phase and the phase sampling signal phase at a rate corresponding to a frequency offset between a frequency of the data sampling signal and a frequency of the received serial data signal so as to frequency synchronize the data sampling signal to the received serial data signal.

10. (Previously Presented) The system of claim 1, wherein the phase interpolator comprises:

a plurality of reference stages adapted to control individual magnitudes of a plurality of component signals having different phases responsive to the plurality of phase control signals; and

a combining node adapted to combine the plurality of component signals into the interpolated data sampling signal.

11. (Previously Presented) The system of claim 10, wherein the plurality of component signals includes four component signals having successive phases separated at intervals of 90°.

12. (Currently Amended) The system of claim 10, wherein the magnitude of at least one of the plurality of component signals is varied from a zero magnitude value to a maximum magnitude value in accordance with the plurality of phase control signals.

13. (Currently Amended) The system of claim 10, wherein the plurality of phase control signals is subdivided into a plurality of signal sets, each one of the plurality of signal sets being used to control the magnitude of a corresponding one of the plurality of component signals, the phase rotator including a ring of storage elements subdivided into a plurality of ring segments, each one of the plurality of ring segments being adapted to store a corresponding one of the plurality of signal sets, whereby each one of the plurality of ring segments controls the magnitude of a corresponding one of the plurality of component signals.

14. (Currently Amended) The system of claim 10, wherein the plurality of phase control signals is subdivided into a plurality of signal sets, each one of the plurality of signal sets being applied to a corresponding one of the plurality of reference stages, each one of the plurality of reference stages being adapted to control a corresponding one of the plurality of component signals in response to the corresponding one of the plurality of signal sets.

15. (Canceled)

16. (Previously Presented) A method of recovering timing information from a received serial data signal, comprising:

(a) deriving a data sampling signal and a phase sampling signal each having an interpolated phase in response to a plurality of phase control signals, wherein the phase sampling signal is offset in phase relative to the data sampling signal by a predetermined amount;

(b) sampling the received serial data according to the data sampling signal to produce a data signal;

(c) sampling the received serial data according to the phase sampling signal to produce a phase signal;

(d) producing a phase error signal based on the data signal and the phase signal, wherein the phase error signal is indicative of a phase offset between the data sampling signal and the received serial data signal;

(e) producing a rotator control signal based on short-term error processing and long-term error processing of the phase error signal; and

(f) rotating the plurality of phase control signals and correspondingly the interpolated phase of the data sampling signal and the phase sampling signal in response to the rotator control signal.

17. (Previously Presented) The method of claim 16, wherein step (f) comprises rotating the plurality of phase control signals and correspondingly the interpolated phase of the data sampling signal and the phase sampling signal in a direction to reduce the phase offset between the received serial data signal and the data sampling signal.

18. (Currently Amended) The method of claim 16, wherein the rotator control signal is one of a phase-advance, a phase-retard, and a phase-hold signal, and step (f) further comprises:

rotating the plurality of phase control[[s]] signals in a first direction to advance the interpolated phase of the data sampling signal and the phase sampling signal in response to the phase-advance signal;

rotating the plurality of phase control[[s]] signals in a second direction to retard the interpolated phase of the data sampling signal and the phase sampling signal in response to the phase-retard signal; and

preventing the plurality of phase control signals and correspondingly the interpolated phase of the data sampling signal and the phase sampling signal from rotating in response to the phase-hold signal.

19. (Previously Presented) The method of claim 16, wherein each of the plurality of phase control signals is a digital signal.

20. (Currently Amended) The method of claim 16, wherein step (f) ~~futher~~ further comprises rotating the interpolated phase of the data sampling signal and the phase sampling signal to one of a plurality of discrete phase values spanning a phase range of 360°.

21. (Canceled)

22. (Previously Presented) The method of claim 16, further comprising rotating the interpolated phase of the data sampling signal and the phase sampling signal at a rate corresponding to a frequency offset between a frequency of the data sampling signal and a frequency of the received serial data signal so as to frequency synchronize the received serial data signal to the data sampling signal.

23. (Previously Presented) The method of claim 16, wherein step (a) further comprises:

controlling individual magnitudes of a plurality of component signals having different phases responsive to the plurality of phase control signals; and

combining the plurality of component signals into the interpolated data sampling signal and the phase sampling signal.

24. (Previously Presented) The method of claim 23, wherein said controlling step further comprises controlling individual magnitudes of four component signals having successive phases separated at intervals of 90°.

25. (Currently Amended) The method of claim 23, wherein said controlling step further comprises varying the magnitude of at least one of the plurality of component signals from a zero magnitude value to a maximum magnitude value in accordance with the plurality of phase control signals.

26. (Canceled)

27. (Previously Presented) The system of claim 1, wherein the phase error processor comprises a short-term error processor and a long-term error processor, wherein:

the short-term error processor integrates the phase error signal over a relatively short time period to generate a phase adjust signal that responds rapidly to changes in the phase offset between the data sampling signal and the received serial data signal; and

the long-term error processor integrates the phase error signal over a relatively long time period to generate a frequency offset signal that responds slowly to changes in the phase offset between the data sampling signal and the received serial data signal.

28. (Currently Amended) The system of claim 27, wherein the short-term error processor and the long-term error processor[[s]] comprise accumulators.

29. (Previously Presented) The system of claim 27, wherein the phase error processor includes a rotate command generator that generates the rotator control signal based on the phase adjust signal and the frequency offset signal.

30. (Previously Presented) The system of claim 1, wherein the phase sampling signal is offset in phase relative to the data sampling signal by a predetermined amount corresponding to a fraction of a symbol period of the received serial data signal.

31. (Previously Presented) The system of claim 30, wherein the phase sampling signal is offset in phase relative to the data sampling signal by one-half of a symbol period of the received serial data signal.

32. (Previously Presented) The method of claim 16, wherein:

the short-term error processing of step (e) further comprises integrating the phase error signal over a relatively short time period to generate a phase adjust signal that responds rapidly to changes in the phase offset between the data sampling signal and the received serial data signal; and

the long-term error processing of step (e) further comprises integrating the phase error signal over a relatively long time period to generate a frequency offset signal that responds slowly to changes in the phase offset between the data sampling signal and the received serial data signal.

33. (Previously Presented) The method of claim 32, further comprising implementing the short-term error processing and the long-term error processing with accumulators.

34. (Previously Presented) The method of claim 32, wherein step (e) further comprises producing the rotator control signal based on the phase adjust signal and the frequency offset signal.

35. (Previously Presented) The method of claim 16, wherein step (a) further comprises offsetting the phase sampling signal in phase relative to the data sampling signal by a predetermined amount corresponding to a fraction of a symbol period of the received serial data signal.

36. (Previously Presented) The method of claim 35, wherein step (a) further comprises offsetting the phase sampling signal in phase relative to the data sampling signal by one-half of a symbol period of the received serial data signal.